ARC FLASH MITIGATION THROUGH THE USE OF AN ENGINEERED PARALLEL HIGH SPEED SEMI-CONDUCTOR FUSE ASSEMBLY

Paper No. ESW-2015-31

Brad Gradwell, CPEng
Member, IEEE, MIEAust
Hudson McKay Group
GPO Box 3072
Brisbane, Queensland, 4000
Australia
brad.gradwell@hudsonmckay.com.au

Abstract – Current-limiting fuses, in their current-limiting range, reduce the available short-circuit current and clear faults in one-half cycle or less significantly limiting the total electrical energy delivered to a fault. If the arc fault current is large enough for a current limiting fuse to be in its current limiting range, the fuse will dramatically reduce the electrical energy delivered to the arc. The use of parallel high speed semi-conductor fuses for low voltage high current applications provides greater limitation than the equivalent fault current limiting fuse rating. The engineered use of parallel high speed semi-conductor fuses can reduce the electrical energy delivered to the arc to below 1.2 cal\cm^2, a level low enough to allow the implementation of PPE Category 0. The use of parallel high speed semi-conductor fuses in the field requires the use of an engineered assembly. This paper details the development of such an assembly and the difficulties overcome to achieve reliable operations.

Index Terms—Arc flash, fault current limiting, semi-conductor fuses, parallel fuses, IEEE 1584, NFPA 70E, arc flash risk management, arc flash mitigation personal protective equipment (PPE)

I. INTRODUCTION

During the expansion of a Coal Handling and Preparation Plant at a black coal mine located NSW Australia, the owner commissioned a power system analysis\arc flash study of the proposed new installation. This study also focus on limiting the peak fault current at the motor control centers (MCC) by current limiting means. The purpose of limiting the peak fault current was to enable the retention of the existing motor control equipment (<5 years old) even though the new system fault level would exceed their design rating. The successful completion of this task would minimize the capital expenditure needed to replace the existing equipment.

Preliminary studies indicated that fault current limiting could be achieved with a single industrial type current limiting fuse, however arc flash incident energies would remain higher than required. Further investigations indicated that the adoption of modern parallel high speed fuses used in the semiconductor industry could provide a viable current limiting solution which also improved arc flash mitigation.

Significant research was undertaken to understand parallel fuse behavior and product development to engineer a parallel fuse interrupter module which mounts directly on the low voltage (415V) distribution transformer secondary terminals. Continuous improvement of the module and 3rd party standards verification testing over a period of four (4) years resulted in a simple, robust and reliable engineered assembly being adopted in the mining sector as part of the owners arc flash mitigation strategy.

II. WHAT WERE THE DRIVERS FOR THIS APPROACH

The first end user organization of the assembly is a large global miner with a stated safety goal of zero work place injuries. In the highly regulated Australian mining industry it is paramount to maintain an excellent safety record, (electrical) otherwise production activities can be shutdown by statutory decree.

Reviews of USA OSHA data [1] [2] in 2009 indicated that the USA still had high incidents of arc flash injury even though the adoption of IEEE1584 [3] and NFPA70E [4] had been in progress for some years. As a result it was considered important to develop an understanding of why this was the case. One theory put forward was the approach to risk management in regards to this problem. It was observed that the accepted methodology, in both Australia and the USA, was to use IEEE1584 to guide the calculation of the arc flash hazard risk while using NFPA70E guidelines for hazard management through safe work practices, procedural systems and PPE.

Many Australian\New Zealand, (AS/NZ) and European, (IEC) standards over the past decade have become less prescriptive and more risk management

 978-1-4799-4782-9/15/$31.00 ©IEEE 2015

based. This requires a designer, owner, constructor, employer and employee to evaluate risks and take the necessary preventive measures. This general principle puts emphasis on avoiding risks, combating them at the source and taking collective protective measures over individual ones.

IEEE1584 quantifies the risk of human exposure to the energy of an arc event. It is essential to conduct an IEEE1584 based arc flash hazard analysis to provide the required risk data for the risk management framework. The goal of the arc flash risk management framework was to conduct a formal assessment of what other means could be used to reduce arc flash energy before implementing NFPA70E guidelines to select Personal Protective Equipment (PPE).

This methodology was driven by the end users observations that there was a reluctance of electrical trades personnel to wear arc rated clothing. In Australia the ambient temperature and humidity experienced for all but a few months at the majority of mine site locations makes the wearing of arc rated PPE (>4 cals\cm^2) uncomfortable. This lead to the question of what else can be done? It was concluded that with the application of the companies risk management protocol [5] and with strict adherence to the hierarchy of controls other preventive measures would need to be found.

III. Risk Analysis and Management

The risk management protocol hierarchy of controls demands that in order of precedence we control a hazard by:

1. Elimination;
2. Substitution;
3. Engineering Out;
4. Isolation;
5. Administer Procedurally; and finally as a last resort
6. Protect (PPE)

The client organization in this instance determined that procedures and PPE should only be relied on in the case when passive and other measures failed to adequately protect against arc flash risk. On this basis the arc flash hazard assessment should not serve as a means of substituting higher level controls with procedures and PEE, but rather lead us as to other ways to protect workers

Australian\New Zealand electrical equipment design standards are based on IEC standards and these standards have sought to provide passive preventative safety [6] since the early 1970's and anecdotal evidence suggests this has led to lower arc flash incidents in Australia. Examples of these standards and codes are:

- IP codes;
- Forms of segregation;
- Arc containment or venting of switchgear;
- Common standards adoption by industry; and
- Type test conformance verification.

This risk management process also forced a rethinking of protection engineering and coordination principles. Production reliability considerations were often drivers of higher than desirable protection settings. However in Australian industry, if personnel are injured it may possibility take far longer to recover from the incident investigation and resulting loss of productivity than from a slightly uncoordinated loss of power supply where little damage occurs and a small production delay is encountered.

The most important conclusion from the risk analysis process was the decision to concentrate on the development of measures which lowered the incident energy to be less than 1.2 cal/cm^2 thereby obtaining a NFPA70E PPE hazard risk category (HRC), Category 0 and retaining the existing natural fibre (cotton drill) PPE standard used on site.

This lead to the investigation and development of the fault current limiting parallel fuse assembly.

IV. Advantages Of Fault Current Limiting For Arc Flash Mitigation

The advantage of a current-limiting overcurrent protective device is that it limits the peak magnitude of fault current that flows through it by opening within the first half-cycle after fault initiation, before the fault current has a chance to reach its peak value.

Current limiting reduces both the magnitude and duration of a fault current. Limiting the magnitude of the peak fault current serves to:

- Limit the total energy delivered to arcing faults;
- Limit thermal and mechanical stresses created in the system by these faults;
- Reduce the magnitude and duration of the system voltage drop caused by fault currents; and
- Minimize damage and resultant downtime.

V. Fault Current Limiting Fuses Or Fault Current Limiting Circuit Breakers

Are circuit breakers or fuses best suited for a particular application? [7] The answer is that several factors must be taken into account, such as:

1. The risk management profile of the organization, (i.e. Safety always before production,);
2. Organizational commitment to the hierarchy of risk management controls;
3. The level of arc flash mitigation required

(ALARP Tolerance Level);
4. Protection application;
5. Selective coordination;
6. Reliability;
7. Renewability; and;
8. Flexibility.

Items 1 through 3 are risk profile factors whereas Items 4 through 8 are best practice protection engineering principles. If Items 1 through 3 are your organizations priority, a paradigm shift in the strict adherence to protection engineering principles may be required.

Protection practitioners will often cite a circuit breakers superiority over fuses for Items 4 through 8, however any device can be improperly applied and improper use of protective devices is an application issue, not a device type issue.

Current limitation is one of the most important features of modern high speed semi-conductor current-limiting fuses. The same is true of fault current limiting circuit breakers, only that, high speed fuses are more current-limiting and faster-acting making them superior for arc flash mitigation.

From a safety risk management perspective the advantages of current limiting fuses are:

- They are non-mechanical devices and therefore are fail safe in operation;
- They are nonadjustable;
- They require little maintenance;
- They can be precisely and easily coordinated even under short circuit conditions; and
- They are "fool proof".

VI. How Do High Speed Fault Current Limiting Fuses Work To Reduce Incident Energy

Modern day current limiting fuses reduce both the magnitude and duration of a fault current. Current limiting fuses designed to IEC 269 Part 4, and UL 248, must clear a short circuit current in less than one half cycle in its current limiting range, (0.008 seconds @ 60Hz or 0.01 seconds @ 50Hz).

Energy is the integral of power with respect to time, therefore the thermal incident energy from an electric arc is directly proportional to the time of the duration of the arc.

$$E = \int_{t_1}^{t_2} v(t)i(t)\,dt \qquad (1)$$

Clearly from Equation 1, if the time that fault current is allowed to flow is reduced, then the incident energy is reduced.

VII. Where There Lessons That Could Be Learnt From Others

Initially the excitement of a possible solution to the fault current limiting problem as well as providing arc flash mitigation was high. In 1996, Saporita [8] in conjunction with a USA industry group conducted a series of tests (3) which concluded *"that the current limitation provided by modern current limiting fuses provided a real reduction in arc-flash energy and associated temperatures, pressures and let-through energy I^2t"*.

However, our systems modelling indicated that little arc flash mitigation benefit was obtained by a single 3000 ampere fuse link or parallel 1500 ampere fuse links for the fault currents in the system under observation. On further research Doughty, Thomas, Macalady, Saporita and Borgwald [9], in 2000 conducted further testing to quantify the benefit provided by current limiting fuses in reducing arc-flash energy. This research concentrated on testing current limiting fuses to determine the relationship between let-through current and the incident energy second degree burn limit (1.2 cal\cm^2). The results indicated that even if the current limiting fuse was operating in its current limiting zone there was the possibility of a second degree burn to bare flesh at 18in from the fault for lower fault levels.

This further supported our initial conclusions from investigations that although current limiting may be achieved by a single high current fuse there was no guarantee that any arc flash mitigation would have been provided.

This observation lead to the investigation of the behavior of smaller nominally rated current fuses in parallel, and how such a system could be implemented practically.

VIII. Is Paralleling Of Fuses Common Practice

The paralleling of fuses is common practice in high power applications [10]. Examples of paralleling of fuses are:

- High current fuses themselves are constructed of parallel elements;
- In high current applications where a single fuse will not carry the load current, two or more fuses are often deployed;
- Protection in semi-conductor power electronics;
- To maximize heat dissipation and minimize losses; and
- To minimize the different fuse models stocked in end user stores.

As higher current fuse elements use a number of parallel elements, the paralleling of complete fuses is

just an extension of this principle. It has been practice for many years to use fuses in parallel without the need for formal testing of such combinations providing:

- The parallel combinations are of the same type and rating;
- The individual fuse has been subjected to satisfactory testing to the required standards; and
- Manufacturer's application recommendations are applied.

IX. WHY USE HIGH SPEED SEMI-CONDUCTOR FUSES

In high powered semiconductor applications such as AC drives, DC drives, soft starters and inverters, over-current protection of the power electronics is provided by modern high speed semi-conductor fuse interrupters [10]. Power semi-conductors are protected by isolating a faulted circuit before the fault current has sufficient time to reach its maximum value and destroy the semi-conductor junction. Purpose built high speed semi-conductor fuse interrupters exhibit all the characteristics required to significantly reduce incident energy in a power system.

Contrary to their description, high speed semi-conductor fuses do not contain any semi-conductor material. Semiconductor high speed fuse-links have been developed from the methods used to produce industrial fuse-links. However, to minimize the I^2t, peak current let-through and increase arc voltage the fuse-links designs have been modified.

High speed semiconductor fuse-links are primarily for short circuit protection, [11] or what is termed partial range. These devices typically only require 5-6 times their nominal rating to operate.

The current limiting behavior of fuses can be explained by application of Kirchhoff's Voltage Law to the schematic diagram, Fig 1, to obtain the current flowing through the equivalent circuit under fault shown in Equation 2

$$\frac{di}{dt} = \frac{V_S(t) - Ri - v_F}{L} \qquad (2)$$

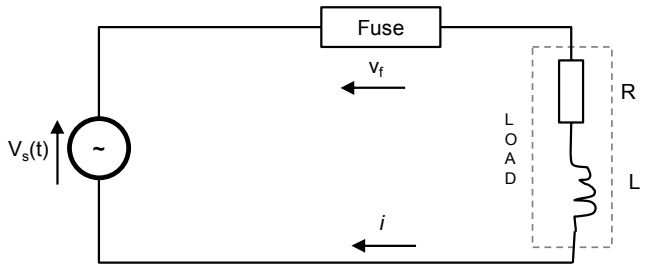

Fig 1 - Equivalent Circuit of Fuse and Connected Load

During the pre-arcing (melting) period the fuse voltage v_F is almost zero and may be neglected, so when the source voltage $V_s(t)$ is positive the circuit current grows with $di/dt \approx Vs\,(t)/L$. When arcing begins v_F increases rapidly and if $v_F > Vs\,(t) - Ri$ the rate of change of current becomes negative and the current is "forced" down towards zero.

The presence of inductance in the circuit prevents the current from changing instantaneously. At the instant the fuse changes its state from the pre-arcing (melting or low-resistance) state to the arcing (high- resistance) state, the current stays almost constant, and the voltage developed across the fuse (arc voltage) increases rapidly.

The higher the arc voltage, the more rapidly the current will be driven to zero during the arcing period. If the design objective for semiconductor fuses is to minimize the let through energy (I^2t), the fuse must be designed to generate a high arc voltage. Semi-conductor fuses are typically operated at more elevated temperatures than other fuse types. Semi-conductor fuse-links also typically operate with higher power dissipations than other fuse types because of the higher element temperatures, often they are also in smaller physical dimension packages. For this reason the body or barrel materials used are often higher-grade materials than those used in other fuse types.

The fuse current waveform has a roughly triangular shape [10], and the total time to clear the fault is the sum of the pre-arcing time and the arcing time.

X. DESIGN CONSIDERATIONS

The design of the parallel high speed semi-conductor fuse interrupter assembly shown in Fig 2 can be broadly categorized in four major tasks:

1. Understanding the theoretical electrical & thermal behavior of the parallel semi-conductor fuses;
2. Designing the fuse holder for the intended thermal and structural performance to AS/NZ [12] and IEC [13] standards;
3. Validating performance in the plant via arc flash analysis; and
4. Performance of the 3rd party independent tests to validate the above.

It was possible to design a reliable parallel current limiting fuse assembly by following the rules below:

- That the manufacturer's published fuse characteristics are used to determine resultant parallel fuse assembly time-current and peak let through curves;
- That the manufacturer's published parallel fuse behavior modifiers be adopted;
- That only fuse links of the same type, size and

resistance (±5%), [11], [14] are applied;
- That connections are as symmetrical as possible to assist in equal current sharing;
- Connections between fuses should be plated copper;
- That the package is factory engineered and installed as a complete unit to comply with the Standards.
- That the nominal current rating, voltage rating and interrupting rating are satisfactory for the load conditions;
- That the time-current characteristic for operating times above 0.01 sec provide proper coordination and selectivity with the load devices and duty; and
- That the current limiting characteristics provide the incident energy reduction required to meet the required PPE hazard reduction category.

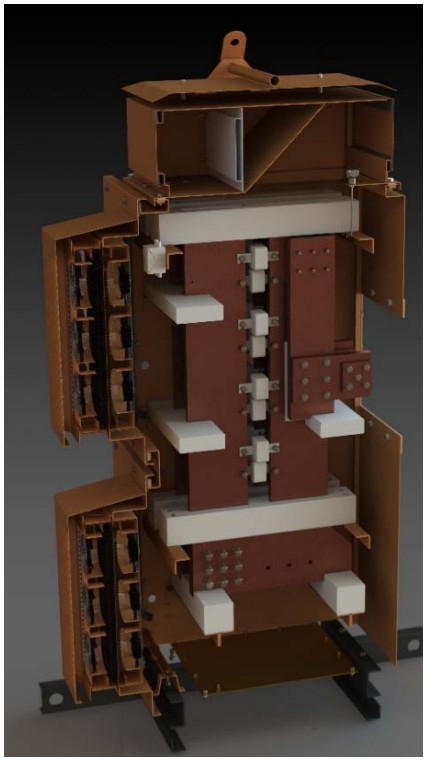

Fig 2 - Cross-section of the parallel fuse assembly [20]

XI. Understanding The Behavior of The Parallel Fuses

A. Determining Nominal Current Rating (I_n)

The maximum permissible load current for a single high speed fuse should be calculated in accordance with the manufactures application guide. Typically the maximum permissible load current is a factor of operating temperature and cyclic overloading. For parallel fuses, manufacturers recommend, [11], [14], [15] using a de-rating factor (df) of:

- 3-4 parallel Interrupters or less the derate factor is 90% of the number of interrupters multiplied by the single interrupter; and
- for more than 4 parallel Interrupters the derate factor is 80% of the number of interrupters multiplied by the single interrupter.

The requirement to derate a fuses based on a number of environmental factors is shown in Equation 2, However the approximation for parallel derating is derived from fact that each individual fuse has an impedance. In a parallel circuit with unbalance impedances in the branches uneven current flow results. The nominal current of the individual fuses in the parallel circuit when summated are derated to prevent premature failure of a single fuse element in the parallel circuit from overcurrent.

In practice the de-rating factor (df) can be calculated using Equation 3

$$df = Fn * Kt * Kv * CD \quad (3)$$

Where

Fn = number of fuses factor (0.9 for n ≤ 4 & 0.8 for n > 4)
Kt = the vendors temperature correction factor
Kv = the vendors cooling air correction factor
CD = the vendors cyclic dimensioning load factor

Appling Equation 3, assuming Kt, Kv and CD = 1, provides a nominal rating for 8 x 500A high speed semi-conductor fuses of 3200A.

B. Time/Current Curve (TCC)

Time current characteristics of parallel high speed fuses can be derived by taking the operating current of the single fuses pre-arcing times, derating and multiplying by the number of parallel paths [11], [14], [15] using:

$$TC_n = TC_1 * n * df \quad (4)$$

Where:

TC_1 = nominal fuse rating time-current characteristics
n = number of fuses in parallel
df = derating factor

In Fig 3 we compare the time current characteristic curves of a single 3000A current limiting Class L fuse and a single 3000A 690V DIN 43 653 high speed semiconductor fuse with the 8 x 500A 690V DIN 43 653 high speed semiconductor fuses [17].

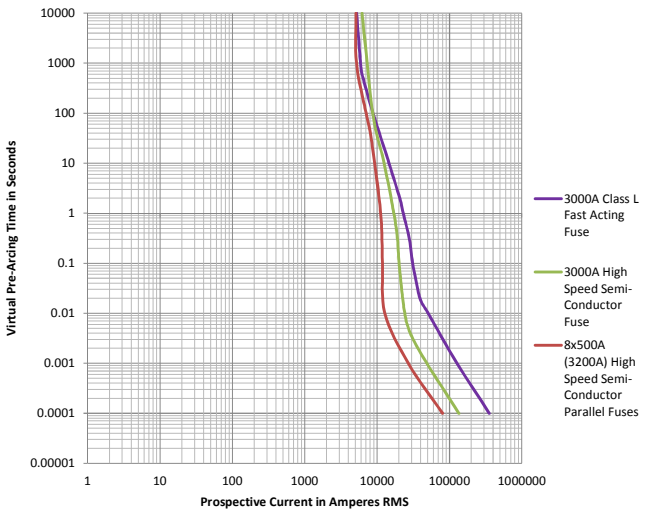

Fig 3 – TCC Comparison between a single Class L 3000A, a HSSC 3000A and 8 x 500A (3200A) parallel HSSC Fuses

From Fig 3, it can be observed that the time current response of the 8 x 500A high speed semi-conductor fuse set is significantly faster than the single 3000A fuses.

C. *Peak Let-Through Current*

The peak let through current of "n" fuses in parallel is $n^{2/3}$ times the peak current of 1 fuse [11], [14].

$$Ip_n = Ip_1 * n^{2/3} \quad (5)$$

Where:

Ip_1 = Nominal Fuse Peak Current
n = number of fuses in parallel

With this in mind the modified Peak Let-Through curve for 8 x 500A 690V DIN 43 653 high speed semiconductor fuses is shown in Fig 4.

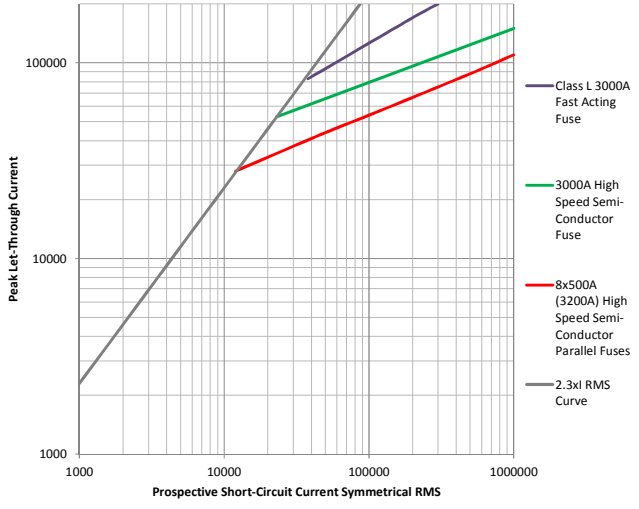

Fig 4 – Peak Let-Through Comparison between a single Class L 3000A, a HSSC 3000A and 8 x 500A (3200A) parallel HSSC Fuses

From Fig 4, it can be observed that the peak let-through current of the 8 x 500A high speed fuses is significantly lower than for the single 3000A fuses. For a circuit with a 15% short-circuit power factor, the instantaneous peak of the available current approximates 2.3 times the rms symmetrical value. The grey line above has a 2.3:1 slope, it can be concluded from Fig 4 that the arc flash incident energy may also be significantly decreased for a fault of corresponding magnitude.

D. *I^2t Characteristics*

At very high currents semi-conductor fuses operate rapidly. The behavior of the fuse at such currents is dependent on the current wave shape and therefore the instant in the voltage cycle that a fault occurs [10]. Therefore when the fuse is operating in its current limiting range the clearance times obtained in Section B. A more suitable measure, which also takes into account the current limiting properties of the fuse, is I^2t. I^2t is the time integral of the square of the instantaneous current through the fuse between the instant of the fault occurring and the instant of clearing the fault as shown in Equation 5.

$$I^2t = \int_0^t i^2 \, dt \quad (5)$$

I^2t is described as the let-through energy of the fuse and at the high currents in the fuses current limiting range this value becomes very constant due to the current limiting effect of the fuse as shown in Fig 5.

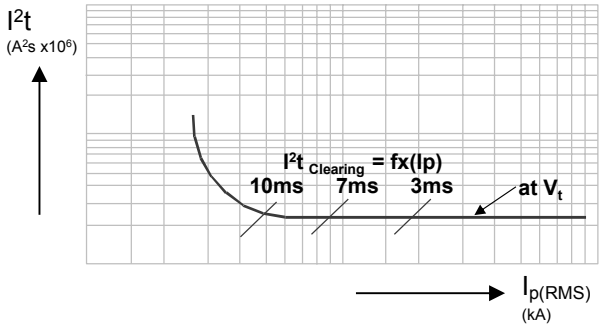

Fig 5 – Typical I^2t Characteristic Curve Showing Constant Let-Through Energy in the Current Limiting Range

Using the same 3000A semi-conductor fuse and the 8 x 500A 690V DIN 43 653 high speed semi-conductor fuses, the total clearing I^2t at rated voltage and at power factor of 15% are given in the published characteristics [16]. For other voltages, the clearing I^2t is found by multiplying by correction factor, K, given as a function of applied working voltage. The voltage correction factor required for operation at 415Vac taken from the correction curve is K = 0.63, [16]. The effect of this adjustment is to lower the let through energy at 415Vac.

For parallel fuses the I^2t of n fuses is n^2 times the I^2t of a single fuse path [11], [14], [15]. Therefore the let through energy of 8 x 500 fuses is 8^2 or 64 times that of a single 500A fuse.

Performing the calculation for both fuses at 415Vac yields the following energy let-through figures at clearing:

- Single 3000A Semi-conductor fuse $I^2t = 8.505x10^6 A^2s$;
- 8 x 500A Semi-conductor fuse $I^2t = 3.830x10^6 A^2s$;

The result above is a paradox as you would logically expect that given the ration between a 3000A semi-conductor fuse and a 500A semi-conductor fuse is 1:6 that the let-through energy for 8 x 500A semi-conductor fuses would be significantly higher than that of the 3000A semi-conductor fuse by up to 64/6 or 10.67 times.

The answer to why a high I^2t has not been obtained with the 8 x 500A semi-conductor fuses in fact lies with the utilization of the semi-conductor fuses with very low I^2t values for their size.

E. Cyclic Loading Considerations

Cyclic loading can lead to premature fuse fatigue. Fatigue occurs if the cyclic loading is of sufficient size and duration to change the temperature of the fuse elements causing weak spots. With careful analysis of the cyclic loading conditions fatigue can be minimized to provide sufficient fuse lifespan and supply reliability to allow programmed replacement of the fuses before "nuisance" failure occurs.

High speed semi-conductor fuse manufacturers provide detail application guides, [18], which give guidance on the assessment of cyclic factors including:

- Influence of overloads; and
- Influence of regular variations in load current.

XII. DESIGN OF THE ASSEMBLY

The design of the fuse assembly essentially consist of two major components:

1. The bus-bar assembly; and
2. The enclosure.

A. Bus-bar Assembly

The bus-bar assembly engineering was completed using an industry design reference publication [19]. The industry publication standard details calculations and procedures for calculating the bus-bar:

- Nominal current rating;
- Impedance;
- Short circuit withstand;
- Temperature rise;
- Voltage drop
- Electromagnetic stresses;
- Recommended joints and connection details; and
- Weight.

These calculations were documented and subjected to internal independent review to ensure accuracy and completeness.

B. The enclosure

The design of the enclosure is more closely related to engineering disciplines normally associated with mechanical and structural engineers. The design of the assembly consists of determining:

- Enclosure strength
- Insulator dielectric and structural strength;
- Cooling and thermal modeling; and
- Standards compliance.

Experienced electrical enclosure design personnel were engaged to develop the enclosure using 3D modeling and applying FEA analysis. In addition experience constructors were extensively consulted to ensure build practicality.

Investigations indicated that there was no standard that could be directly applied to the parallel fuse assembly under design. In absence it was decided to adopt the practices detailed in AS3439 Low Voltage Switchgear and Control Gear Assemblies.

XIII. INDEPENDENT TESTING TO AS/NZ AND IEC STANDARDS

Type testing was performed by the TUV, NATA certified test center located in Melbourne Victoria Australia during June 2010 through to September 2012. The testing program was conducted in accordance with:

- AS\IEC60947.1 Low Voltage Switchgear and Control Gear – General Rules; and
- AS3439.1 Low Voltage Switchgear and Control Gear Assemblies

The tests performed included:

- Short Circuit Test;
- TCC Validation;
- Dielectric Tests;
- Temperature Rise; and
- Arc Fault Containment.

A series of formally certified and internationally recognized test reports collating the results and oscilloscope traces for the above have been issued.

A. Short Circuit & TCC Validation Type Test

The interrupter was connected to the high current test rig, Figure 6, and with the load side of the interrupter

shorted between phases, subjected to short circuit testing at 63kA, 40kA, 20kA, 15kA, 13kA and 12kA at 415Vac, 50Hz.. These tests were carried where possible three times at each level to gauge repeatability of the results.

Fig 6 – High Current Test Rig

The results of the short circuit withstand tests are shown below in Fig 7. The 6.25kA test was carried out using the low voltage temperature rise test rig due to the connection times involved. For example the 3200A rated interrupter was subjected to 5kA for 40 minutes without operation of the fuse. However at 6.25kA operation occurred in approximately 6 minutes.

Peak Let Through Current								*Time (s)*			
Test Current	Red Phase Current	White Phase Current	Blue Phase Current	Max Current	STD Dev	Average	% Dev	Red Phase Clearing Time	White Phase Clearing Time	Blue Phase Clearing Time	Max Clearing Time
63000	28300	34300	28300	34300	230.9401	34550	0.668%	0.0058	0.0037	0.0058	0.0079
63000	26300	34500	17300	34500				0.0079	0.0036	0.0079	
63000	27400	34700	27500	34700				0.0063	0.0039	0.0063	
63000	28300	34700	28400	34700				0.0058	0.0039	0.0059	
43000	27000	31900	27200	31900		31900		0.007	0.0046	0.007	0.0070
20500	24450	26600	14000	26600	513.1601	27167	1.889%	0.01	0.0059	0.01	0.0104
20500	23700	27300	15400	27300				0.0104	0.0062	0.0104	
20500	23700	27600	27600	27600				0.0095	0.0065	0.0095	
15500	27200	23600	21700	27200	208.1666	27133	0.767%	0.0097	0.0162	0.0162	0.0162
15500	27300	22700	22700	27300				0.0095	0.0162	0.0162	
15500	26900	24100	12500	26900				0.0104	0.0127	0.0127	
11200										5.53	6.0600
11200										5.59	
11200										6.06	
6250								303.6		366	366.00
4500								2400		3000	3000.00

Fig 7 – Tabulated Characteristic Validation Results, ITACS\TUV Test Report No 1530

From Fig 7 it can be concluded that the parallel interrupters provided under test:

- Repeatable characteristics given the small test sample evidenced by the small % deviation;
- Fault current limiting for rms fault currents greater than 20.5kA evidenced by the interruption in less than 0.01 seconds.

The results contained in Fig 7, are then plotted against the theoretical Peak Let-Through curve, Fig 8 and the Time Current curve, Fig 9. Fig 8 and Fig 9 also indicate a close correlation exists between theoretical behavior and observed behavior.

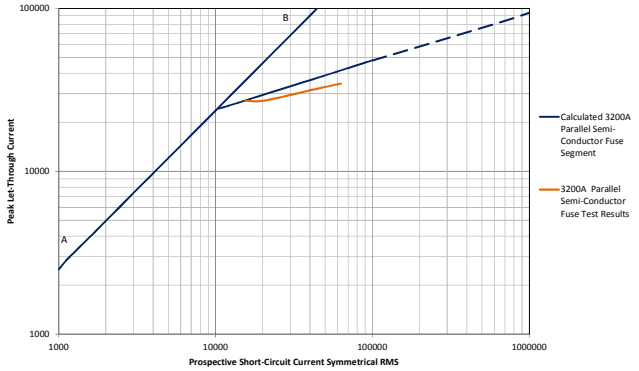

Fig 8 – 8 x 500A Interrupter, Peak Let-through, Calculated vs Test Clearing Time

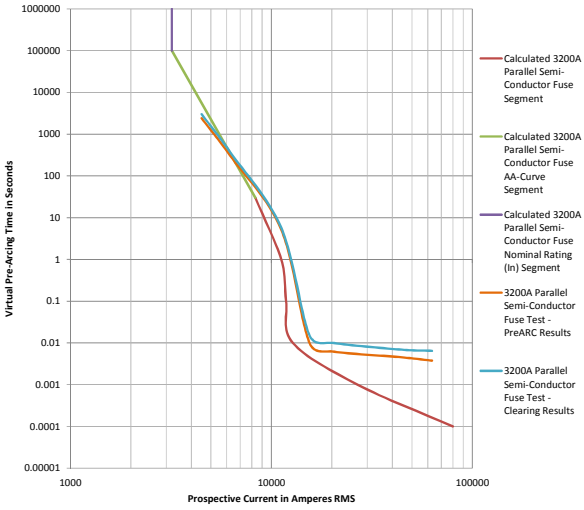

Fig 9 – 8 x 500A Interrupter Time Current Curve, Calculated Pre-Arc vs Test Clearing Time

The clearing I^2t test results are tabulated below in Fig 10.

I^2T ($x10^6$)							
Test Current	Red Phase	White Phase	Blue Phase	Average	STD Dev	Average	% Dev
63000	1.41	1.49	1.22	1.373333	0.053886	1.489167	3.619%
63000	2.39	1.85	0.99	1.743333			
63000	1.33	1.65	1.42	1.466667			
63000	1.32	1.61	1.19	1.373333			
43000	1.52	1.59	1.38	1.496667		1.496667	
20500	1.91	1.75	0.633	1.431	0.229067	1.629222	14.060%
20500	2.03	1.87	0.83	1.576667			
20500	2.39	1.88	1.37	1.88			
15500	2.42	3.95	1.95	2.773333	0.716987	2.454444	29.212%
15500	2.54	3.96	2.37	2.956667			
15500	2.21	2.15	0.54	1.633333			

Fig 10 – Tabulated I^2t Results, ITACS\TUV Test Report No 1530

Using the calculation of the average clearing I^2t at each test current, Fig 11, demonstrates that limiting of let through energy at a constant value occurs for short circuits greater than 20kA.

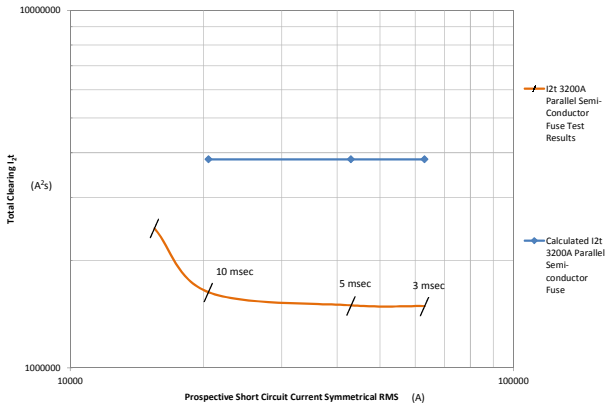

Fig 11 – 8 x 500A I^2t Characteristics

From Fig 11 it can be seen that the test results were a factor of three lower than expected. However we believe this is a result of the unequal impedance paths causing one fuse to interrupt faster, (initially carries significant more fault current) and then a rapid cascading effect occurs. To prove this theory, during our testing we carried out a balanced fuse impedance test, Fig 7 & Fig 10 63000A, test 2, and the interrupter took longer to operate and had a higher I^2t let through closer to the calculated results than a random selection of fuses validating the basis of our theory.

B. Temperature Rise Type Test

During the initial phases of the development, the client required an IP56 rated enclosure. This would require the units to be sealed and hence any heat generated would be contained in the enclosure. To ensure that the module operated reliably and no nuisance operations would be experienced temperature rise type testing was carried out. The aim of this testing is to ensure that temperatures of the components of the module remain within prescribed limits. The test rig is shown in Fig 12 and the measurement points shown in Fig 13.

Fig 12 – Temperature Rise Current Injection Test Rig

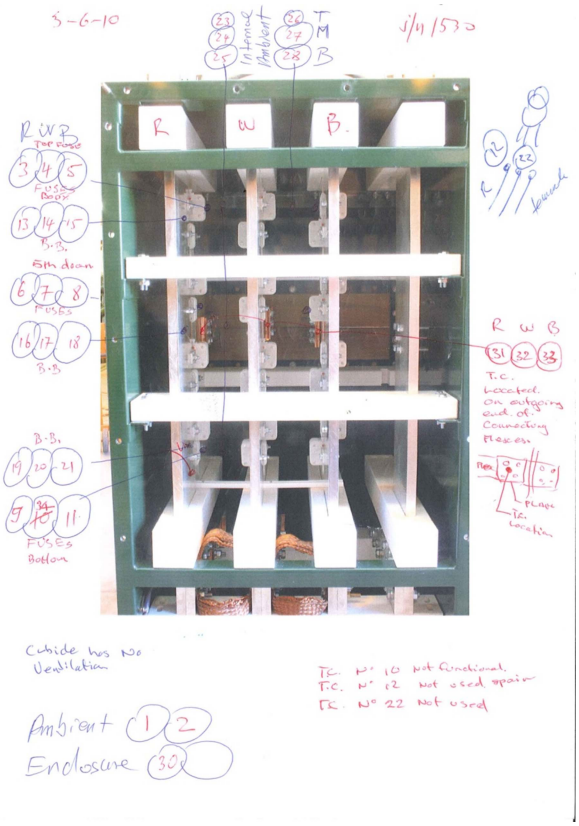

Fig 13 – Temperature Rise Measurement Points

This test at full load rated current, (3200A) proved problematic with thermal runaway conditions observed, Fig **14**, which fails the prescribe test limits and continued operation at these temperatures was likely to cause premature failure of the interrupters.

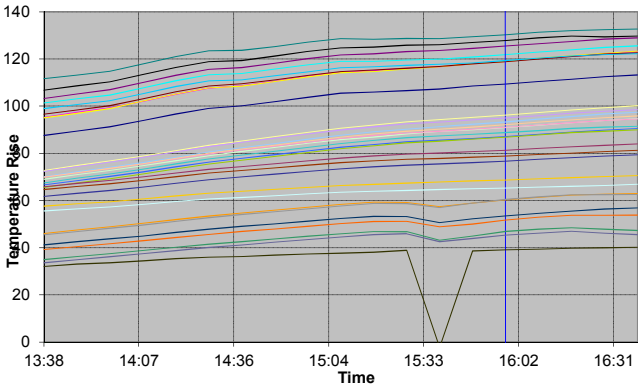

Fig 14 – Temperature Rise Results (Failed Test)

On further investigation, the inducing of air flow around the high speed interrupters could dramatically improve the test results shown in Fig 14. However, we were required to maintain an IP56 rating and after several prototypes a cooling system was devised and subjected to the same testing. The final module design is shown in Fig 15 and the pass results shown in Fig 16 indicate reaching of equilibrium at less than 1 ºC/Hr movement in measured temperatures.

Fig 15 – IP56 Module Undergoing Temperature Rise Test

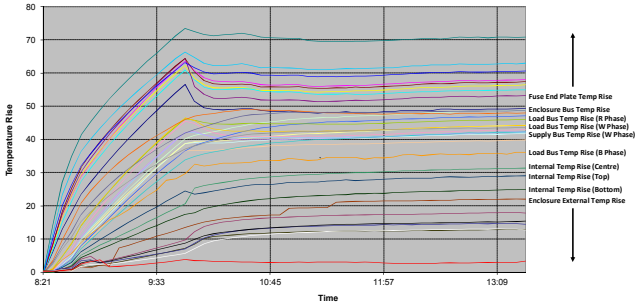

Fig 16 – Successful Temperature Rise Results, TUV Rheinland Test Report No 19300582005

The tests above were carried at an ambient temperature of 25ºC and a maximum module internal temperature of 56ºC degrees was obtained. The maximum rise on the fuse end plates reached 70ºC. Given that the manufacturer's maximum allowable rise is 110ºC this left margin for higher ambient temperatures. Extreme ambient temperatures of 45-50 ºC can be experienced in many parts of Australia and equipment specifications often require operation between -5 ºC to 45 ºC. Simulation of direct radiant heat, simulating the sun falling directly on the cooling heat exchangers, is shown in Fig 17 and the results shown in Fig 18.

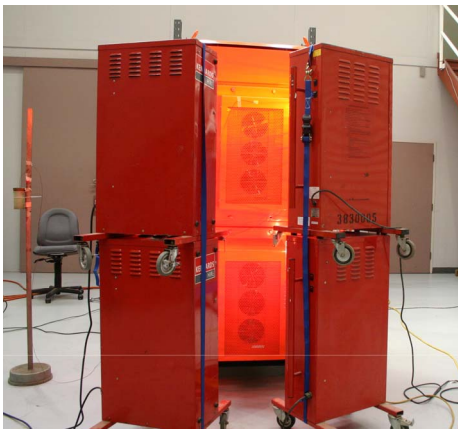

Fig 17 – IP56 Module Undergoing Extended Temperature Rise Test

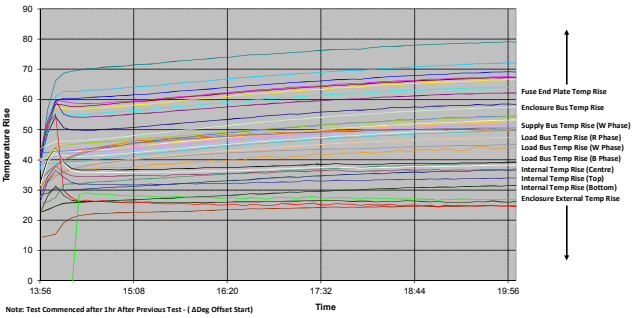

Fig 18 – Successful Extended Temperature Rise Results, TUV Rheinland Test Report No 19300582006

The ambient temperature reached 34ºC with a maximum internal temperature of 73ºC and maximum rise on the fuse end plates reached 67ºC. Reaching of equilibrium at less than 1 ºC/Hr movement is achieved which indicates that the rising effects of ambient temperature on the module are linear.

C. Arc Fault Containment Type Test

To assess the safety of personnel standing in front of the module the unit was subject to the prescribed [13] arc fault containment test shown below in Fig 19.

Fig 19 – IP56 Module Undergoing Arc Fault Containment Test, TUV Rheinland Test Report No 19300582004

The arc fault containment test requires the input bus-bars to be shorted and current is introduced. The resultant explosion should be contained sufficiently within the module and vented in a manner that preserves the cloth strung at the front of the module. The protective device was set to open in 200ms. However due to the nature of the arc blast travelling across the primary bus to the secondary bus the fault was cleared within 30ms without setting the cloth on fire. The observation of this result is that the initiated arc was blown across from the primary bus-bar section to the secondary bus-bar section and the fuses interrupted the arc current further validating previous observations of the modules ability to interrupt even under low fault conditions.

XIV. MODELING OF THE ASSEMBLY

It was concluded that a prudent, systematic and conservative approach be adopted when modelling and specifying the parallel high speed interrupters. This structured approach, was completed for every installation. Each individual installation is unique as the impedance of the source, distribution transformer, MCC feeder cable, loads and load feeders all affect the effectiveness of the interrupters ability to reduce arc energies.

XV. APPLIED INDUSTRY EXAMPLE

The aim in this installation was to provide:

- Fault Current Limiting to less than 50kA 3 sec; and
- Arc Flash Mitigation to <1.2 cal\cm^2 with a maximum hazard classification of PPE Category 0.

Initial modelling of the MCC, Fig 20, indicated that at the MCC busbar the incident energy would be >40 cal\cm^2 producing a PPE Category “Dangerous” and at the MCC incomer the incident energy 5.7 cal/cm^2 indicated a PPE Category 2 within the MCC cells and near in faults.

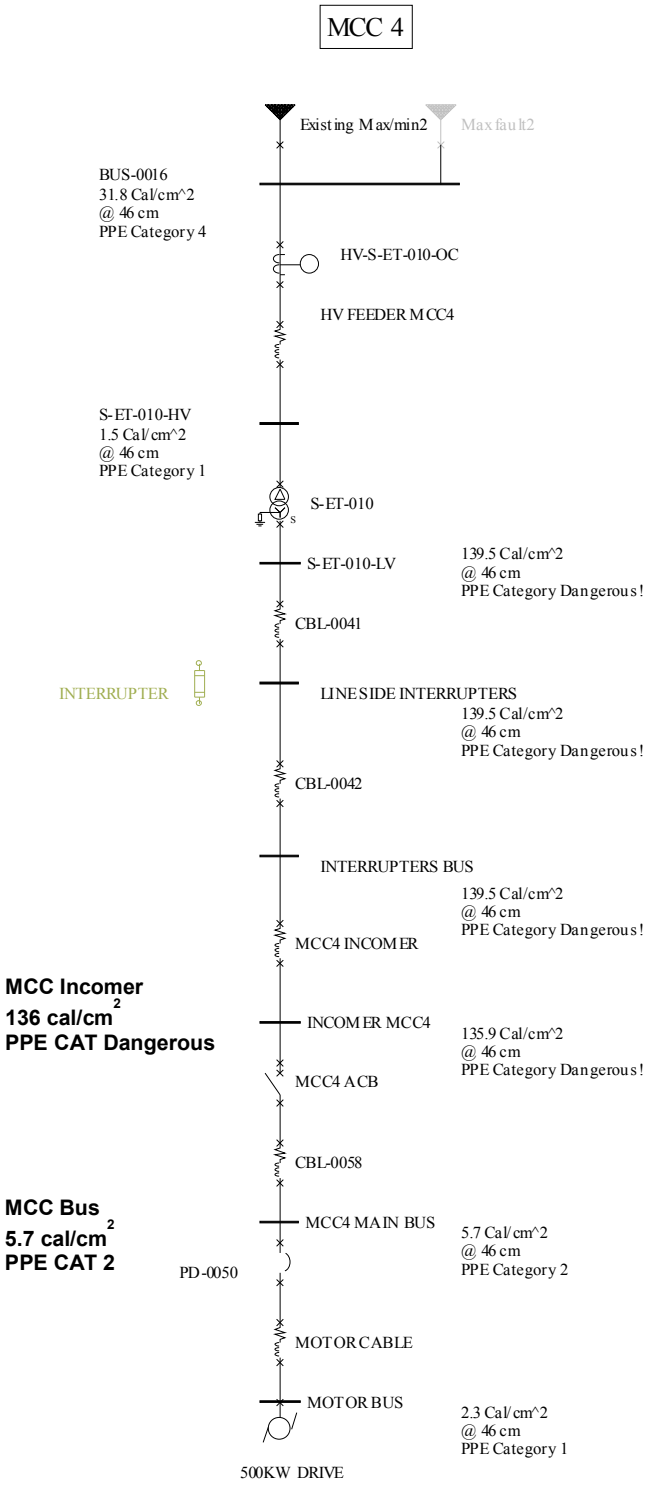

Fig 20 – Software One Line with no Interrupter Mitigation

With the addition of parallel interrupters, Fig 21, the

resultant incident energy was reduced to below 1.2 cal/cm^2 at the MCC incomer and the MCC cells allowing the adoption of PPE Category 0.

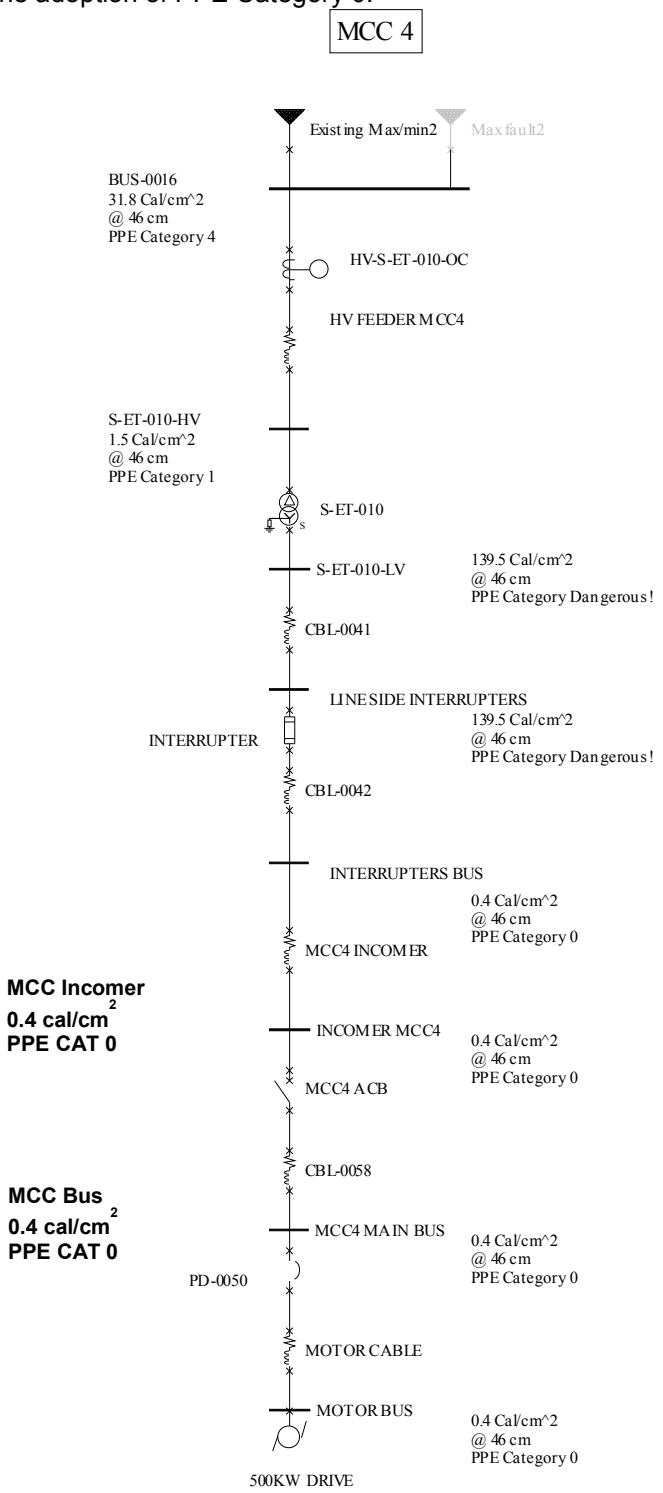

Fig 21 – Software One Line with Interrupter Mitigation

The scheme also provides peak current limiting and with a prospective fault current of 58.41kA before the parallel interrupter module the peak let through current is 40kA, Fig 22. This equates to a maximum prospective rms fault current at the MCC of approximately 18kA and would allow the MCC's with a rating of 50kA to be retained.

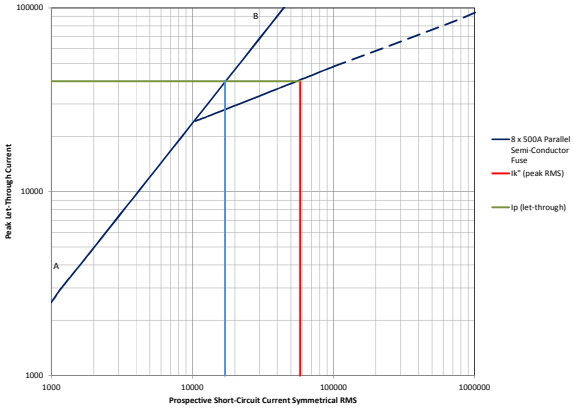

Fig 22 – MCC4 prospective fault current after Interrupter's are installed

To further assess the reliable "in service" operation of the interrupter, verification of coordination during MCC preload and the largest motor starting was required. Fig 23 shows the coordination obtained by a 500kW drive started DOL while Fig 24 shows the coordination with a 500kW drive started with a VVVF drive.

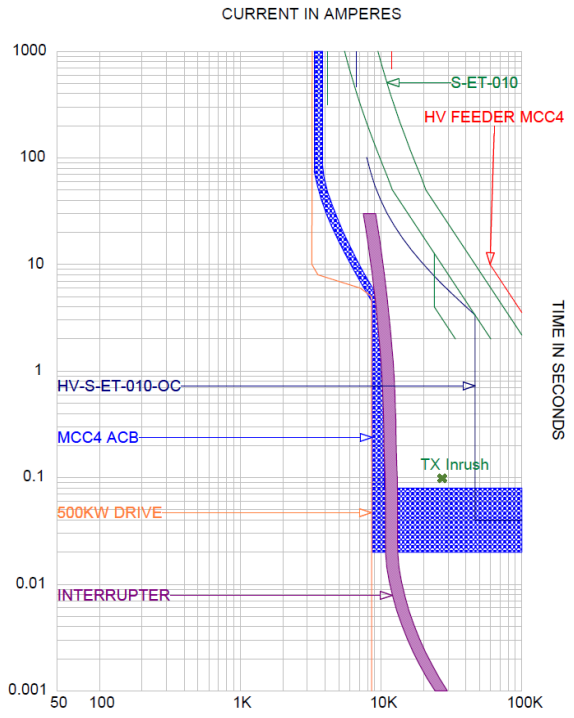

Fig 23 – MCC TCC with Interrupter Mitigation and 500kW DOL Motor Start

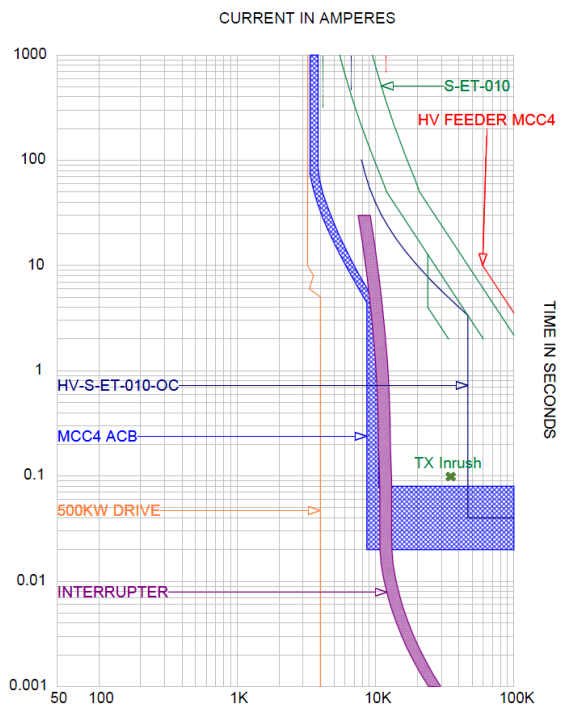

Fig 24 – MCC TCC with Interrupter Mitigation and 500kW VVVF Motor Start

From the analysis of the results obtained during these investigations, the required design features were achieved with parallel high speed fuse interrupters, That is:

- Current limiting allowing the use of the existing infrastructure.
- Arc flash hazard mitigation achieved an incident energy below 1.2 cal\cm^2 with an assessed PPE Category 0; and
- Reliable operation at nominal load current of the plant.

As a result, the global mining company authorized the construction and installation of five 3200A parallel interrupter modules and has adopted the installation of the parallel interrupters as part of the arc flash hazard mitigation strategy.

XVI. Summary of the Development Journey

This paper is the result of a five year journey to develop a reliable and robust solution for arc flash mitigation at a global mining company. It commenced in early 2009 with an arc flash study and morphed into a product development cycle. The electrical principles and basic bus-bar design has not changed significantly since 2010. What was required to change over this time was the maturity of the enclosure and thermal management system design in order to pass the temperature rise type test requirements.

Parallel interrupter modules of various sizes have been in reliable operation for up to 5 years, this includes:

2 x 3600A (3MVA Restricted) IP56 Units Forced Cooled;
1 x 3200A (3MVA Restricted) IP56 Units Forced Cooled;
6 x 3200A (3MVA Restricted) IP56 Units Natural Cooled;
4 x 2MVA IP56 Units Forced Cooled;
2 x 1.5MVA IP56 Units Forced Cooled; and
1 x 750kVA IP56 Unit Forced Cooled.
2 x 500kVA Sealed IP56 Units
5 x 500kVA Air Cooled IP2x Units (Mining Electric Shovels)

In that time there has been two operations preventing equipment damage and/or injury, one from an excavator digging and causing accidental cable damage and secondly from a VVVF drive harmonic filter failure which prevented complete destruction. This journey is summarized below in figures.

Fig 25 – First 3200A Module - 2009

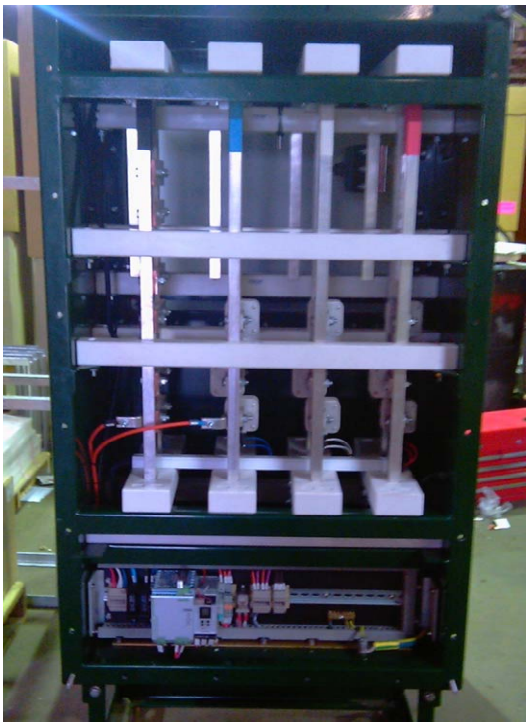

Fig 26 – Prototype 750kVA Forced Cooled Module – 2010

Fig 27 – 2MVA Forced Cooled Module 2011

Fig 28 – 500kVA Air Natural Module – Electric Shovel – 2011

Fig 29 – 3200A Forced Cooled Module - 2012

Fig 30 – 500KVA IP56 Module - 2012

XVII. Conclusion

The adoption of parallel fuses is common practice and the theory behind their behavior is well documented and available in the public domain.

Parallel high speed semi-conductor fuses operating in their current limiting range provide improved peak current limiting over single fuses of the same nominal value which reduces incident energy available for arc flash. Modelling, testing and "in service" operation shows that with careful selection and design application, parallel high speed semi-conductor fuses operating in their current limiting range can reduce arc flash incident energies to below 1.2 cal\cm^2 allowing the adoption of PPE Category 0 in low voltage installations while maintaining reliable energy supply for production activities.

Acknowledgment

The author gratefully acknowledge the contributions of, C. Nicholls for his effort and dedication to designing the prototype, P. Cameron for the hours of modelling and T. Clark and Peter Floyd for their faith, support and calculated risk taking as the end user.

References

[1] OSHA, "Census of Fatal Occupational Injuries 1992-2002," *USA*, Available: http://stats.bls.gov/iif/oshcfoi1.htm

[2] OSHA, "Census of Fatal Occupational Injuries 2008," *USA*, Available: http://stats.bls.gov/iif/oshcfoi1.htm

[3] *IEEE Guide for Performing Arc-flash Calculations,*, IEEE Standard 1584-2002.

[4] *Standard for Electrical Safety Requirements for Employee Workplaces,*, NFPA 70E, 2000

[5] *Risk Management*, AS\NZS 4360, 2004

[6] J. Vrielink, H. Picard and W Wittleman, "Common Sources of Arc Flash Hazard in Industrial Power Systems," in *Proc. 2011 IEEE Petroleum and Chemical Industry Europe Conference.*

[7] T, Parsons. A Comparison of Circuit Breakers and Fuses for Low Voltage Applications. Data Bulletin *Schneider Electric.* [Online] Available:http://static.schneider-electric.us/assets/consultingengineer/appguidedocs/0600DB0601.pdf

[8] V Saporita. "Using, Current-Limiting Fuses to Reduce Hazards Due to Electrical Arc-Flashes". *Cooper Bussmann.* [Online] 1996. Avalable : http://www.arcwear.com/articles/pdf/Current-LimitingFuses.pdf.

[9] R.L. Doughty, T.E Neal, TL Macalady, V Saporita and K Borgwald **.** "The use of low-voltage current-limiting fuses to reduce arc-flash energy.", *Industry Applications, IEEE Transactions on , vol.36, no.6, pp. 1741- 1749.* [Online] 12 2000. Avalable :http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=887229&isnumber=19171.

[10] A Wright and P.G. Newbery, *Electric Fuses*, 3rd Edition. Stevenage Herts: The Institution of Engineering and Technology, 2012, pp. 42-43, pp72-76, pp87-88, pp108, pp171-182, pp220-227.

[11] High Speed Fuses Applications Guide. *Cooper Bussmann.* [Online] Avalable : http://www.cooperbussmann.com/pdf/e117a412-79c0-436e-943e-969a1f80ad6e.pdf.

[12] *Low-voltage switchgear and controlgear assemblies - Type-tested*, AS\NZS 3439.1 & .3 - 2002

[13] *Low-voltage switchgear and controlgear*, IEC\AS\NZS 60947.1 &.2 - 2005

[14] C. Mulertt, EduPack Paralleling Fuses, GP109-Paralleling Fuses. *Ferraz Shawmut.* [Online] 29 09 2004. Avalable : http://www.bezpieczniki.com/strony/artykuly/ferraz/GB109_Paralleling_fuses.pdf or as a presentation at: http://ep-uk.mersen.com/fileadmin/user_upload/_common_/Training_Modules/TM_109_Parallel_Implentation_Of_The_Fuses_EN.pdf

[15] Application Information For High Speed Fuses Edison/*Cooper Bussmann.* [Online] Avalable : http://edisonfuses.net/Edison/EDISON_FUSES_APPLICATION.pdf

[16] BIF Document #17056320, DIN 43 653 Electrical Characteristics. *Cooper Bussmann.* [Online] 7 11 01. Avalable :: http://www.cooperbussmann.com/pdf/720014.pdf.

[17] BIF Document #720014, Typower Zilox Characteristics. *Cooper Bussmann.* [Online] 7 11 01. Avalable :: http://www.cooperbussmann.com/pdf/720014.pdf.

[18] High Speed Fuse Application Guide/ *Cooper Bussmann.* [Online] Avalable : http://www.cooperindustries.com/content/dam/public/bussmann/Electrical/Resources/technical-literature/High_Speed_Fuse_Application_Guide.pdf

[19] Publication 22 – Copper for Bus Bars, *Copper Development Association.* [Online] 7 11 01. Avalable :: http://www.copperinfo.co.uk/busbars/pub22-copper-for-busbars/homepage.shtml

[20] Australian Innovation Patent No. 2011101542 in the name of PACE Engineers Group Pty Ltd - "ARC FLASH PROTECTION APPARATUS" - Divisional of International Patent Application No. PCT/AU2010/001350 filed 13 October 2010

Vita

Brad Gradwell has over 32 years electrical industry experience having completed an Electrical trade's certificate in 1986, Electrical apprenticeship in 1987, Electrical Engineering Diploma in 1988, Bachelor Engineering (Hons) – Electrical Power & Control 1996 and a Masters of Engineering in 2000. Over this time he has worked in Power Generation, EHV Switchyards, Aluminum Smelting, Mining and Ports Infrastructure. He is a Chartered Professional Engineer in Australian and currently Managing Director of Hudson McKay Group overseeing its design and construct operations.